DESCRIPTION

TITLE OF THE INVENTION

Power Transistor Protecting Circuit of Motor Drive Circuit, Motor Drive Circuit and Semiconductor Device

TECHNICAL FIELD

[0001]

The present invention relates to a power transistor protection circuit of a motor drive circuit, a motor drive circuit and a semiconductor device and, in particular, the present invention relates to a power transistor protection circuit of a motor drive circuit of, for example, a unipolar (half wave) drive stepper motor, capable of preventing a power transistor from broken when a connection between an output terminal of the power transistor and an exciting coil of the motor is broken.

BACKGROUND ART

[0002]

In a unipolar drive stepping motor driver (pulse motor driver), a gear-shaped rotor is rotated step-by-step by a predetermined angle by sequentially driving a stator of the stepping motor by a single phase drive, a single phase-two phase drive or a two phase drive, etc.

The driver for supplying drive current for driving the stator sequentially includes exciting coils provided on the stator and connected to a power source line and power transistors (output stage transistors) provided for respective phases and connected in series with the respective

exciting coils. The stepping motor is driven by sequentially exciting the exciting coils of the stator by ON/OFF control of the power transistors with a predetermined timing.

When the power transistor of a certain phase is turned ON, the drive current is sequentially increased in the ON period due to transient phenomenon of a predetermined time constant determined by inductance of the exciting coils in the same phase and impedance of the power transistors, etc. In order to limit the increase of the drive current to a predetermined value, the power transistor is turned ON and, after a predetermined time lapses from the turning ON, turned OFF so that an over current does not flow through the power transistor. In order to realize the scheme, the power transistor is driven such that each phase is chopped logically by pulses of HIGH level "H" and LOW level "L".

[0003]

As an example of such pulse drive control, a protective circuit for a three phase motor drive, which is chopper controlled by setting an ON period by a timer circuit, and an integrated gate bipolar transistor (IDBT) thereof are well known (Patent Reference 1).

Patent Reference 1: JPH11-112313A

DISCLOSURE OF THE INVENTION

PROBLEMS THAT THE INVENTION IS TO SOLVE

[0004]

A power transistor protective circuit such as described is generally an over-current protective circuit or a current limiter circuit. However, when the motor driver is provided in an IC, terminals of exciting coils of the motor are connected to

output terminals of the IC. Therefore, the connection between the output terminals and the motor tends to be broken. Further, the exciting coils tend to be broken due to the existence of the rotor.

Further, in the motor drive circuit, there may be a case where one of the output terminals of the power transistors is instantaneously opened due to noise and/or driving state of the motor. Therefore, when the breaking of the connection is detected by detecting the open state of the output terminal, error tends to occur and influence the driving operation of the motor drive circuit, so that this countermeasure is not realistic. Accordingly, there is no such protection circuit.

In the stepping motor driver, the drive of the motor continues even when the breaking of one of the output terminals or the breaking of the exciting coils occurs. In such case, counter-electromotive force is not generated in the exciting coil connected to the open terminal. Therefore, currents flowing in other exciting coils are increased correspondingly and the drive of the motor is continued under overload condition. Thus, the power transistors may be broken and the IC itself may be broken.

The present invention is intended to solve the problem of the prior art and an object of the present invention is to provide a power transistor protective circuit of a motor drive circuit, a motor drive circuit or a semiconductor device, which is capable of preventing a power transistor from being broken when there is a breaking on a side of an output terminal of the power transistor, which is connected to one terminal of the exciting coil, or on a side of the other terminal of the exciting coil.

MEANS FOR SOLVING THE PROBLEMS

[0005]

In order to achieve the above object, a power transistor protective circuit of a motor drive circuit, which includes power transistors provided correspondingly to exciting coils of a motor and supplying drive currents to output terminals of the motor driver circuit, which are connected to one terminals of the respective exciting coils, according to a first aspect of the present invention, comprises a terminal open detection circuit, a breaking detection circuit and a drive suspension circuit.

The terminal open detection circuit is provided correspondingly to each of a plurality of power transistors and provided between one of a side of said output terminal and a line connected to said output terminal and one of a side of the other terminal of said exciting coil and an other line connected to the other terminal and, one of the output terminals connected to one terminal of one of the exciting coils and the other terminal of the exciting coil and, when the power transistor is supplying a drive current to the output terminal connected to the one terminal of the exciting coil, the terminal open detection circuit determines whether or not there is an open state or a closed state between one of the side of said output terminal and the line connected to said output terminal and one of the side of the other terminal of said exciting coil and the other line connected to the other terminal.

The breaking detection circuit detects a breaking state or a non-breaking state, when the terminal open detection

circuit detects a non-open state and then an open state between one of the side of said output terminal and the line connected to said output terminal and one of the side of the other terminal of said exciting coil and the other line connected to the other terminal.

The drive suspension circuit suspends the driving operation of the motor drive circuit when the breaking detection circuit detects the breaking state.

According to a second aspect of the present invention, the terminal open detection circuit detects an open state or a closed state on the side of the output terminal of the power transistor protective circuit or on the side of the other terminal of the exciting coil when the power transistor is outputting the drive current.

The braking detecting circuit detects a breaking state when a plurality of open states are detected correspondingly to the detection of the open state or the non-open state by the terminal open detection circuit.

ADVANTAGE OF THE IVENTION

[0006]

In the first aspect of the present invention, when the power transistor is outputting the drive current, the terminal open detection circuit determines whether or not there is an open state or a closed state between one of the side of said output terminal and the line connected to said output terminal and one of the side of the other terminal of said exciting coil and the other line connected to the other terminal. Further, the terminal open detection circuit detects the non-open state and then the open state.

As such, according to the first aspect of the present invention, the detection of the non-open state on the side of the output terminal or on the side of the other terminal of the exciting coil and then the detection of the open state are performed every output operation of the drive current of the power transistor to detect a change from the non-open state to the open state. Further, according to the first aspect of the present invention, by using the non-open state and the open state as detecting condition, it is substantially determined whether or not the open state continues until a next drive current supply.

On the other hand, according to the second aspect of the present invention, the terminal open detection circuit detects the open state or the closed state on the side of the output terminal or the side of the other terminal of the exciting coil during the power transistor is performing the drive current output. The braking detecting circuit detects a breaking state when a plurality of open states are detected correspondingly to the detection of the open state or the non-open state by the terminal open detection circuit.

Incidentally, in the above mentioned detections, the non-breaking state is the open state and the non-open state is the closed state.

By judging the breaking state under these conditions, there is no breaking detection error and it is possible to reliably detect the breaking without influence on the drive operation of the motor drive circuit. Thus, it is possible to suspend the drive operation of the motor drive circuit when the breaking occurs.

Further, by always detecting the open state or the

non-open state when the power transistor is outputting the drive current, the detection is not influenced by instantaneous noise or change of the driving state. Particularly, by determining whether or not the open state exists with using a voltage close to the voltage corresponding to the limit current of the drive current, it is possible to detect the open state without influence of instantaneous noise or instantaneous change to the open state.

As a result, it is possible to immediately detect a breaking occurring on the side of the output terminal of the power transistor connected to the one terminal of the exciting coil or on the side of the other terminal of the exciting coil, so that it is possible to prevent the power transistor from breaking.

BEST MODE FOR CARRYING OUT OF THE INVENTION

[0007]

Fig. 1 is a block circuit diagram of a stepping motor driver, which has a plurality of power transistor protective circuits, of a unipolar drive stepping motor to which a power transistor protective circuit of a motor drive circuit according to an embodiment of the present invention is applied and Fig. 2 is a timing chart of an operation of the power transistor protective circuit.

In Fig. 1, a unipolar drive stepping motor driver IC 10 includes current output circuits 1a, 1b, 1c and 1d, which have output terminals 2a, 2b, 2c and 2d connected to single phase exciting coils 11a, 11b, 11c and 11d of a stepping motor 11, respectively.

The exciting coils 11a, 11b, 11c and 11d are connected to

a power source line 13 of a power source (battery) 12. Incidentally, flywheel diodes D are connected in parallel to the exciting coils 11a to 11d, respectively.

The power source 12 supplies power to a voltage regulator circuit (REG) 2 provided within the IC through a terminal 2e and the REG 2 applies a stabilized voltage, for example, 3V, to an internal power source line +VDD to thereby supply power to various circuits provided internally of the IC.

The single phase drive circuits 1a to 1d have identical circuit constructions and, therefore, only the current output circuit 1a is shown and described in detail.

[0008]

The single phase drive 1a is constructed with an N channel MOSFET power transistor 3, a power transistor protective circuit 4, a current limiter circuit 5 and a reference voltage generator circuit 6. Incidentally, for simplicity of description, the current limiter circuits 5 of the respective single phase drive circuits are shown outside of the single phase drive circuit 1a.

The power transistor 3 has a drain connected to the output terminal 2a to output an exciting current to the output terminal 2a. A source of the power transistor 3 is connected to a resistor Rs provided externally of the IC through a terminal 2f. The resistor Rs is provided between the terminal 2f and ground and used to detect an output current. Incidentally, the output current of the output terminal 2a is a sink current from the exciting coil 11a.

The power transistor protective circuit 4 is constructed with a terminal open detection circuit 4a for detecting an open state between the power source line 12a of the power source 12

and the output terminal 2a and a circuit breaking detection circuit 4b.

The terminal open detection circuit 4a detects the open state between the output terminal 2a and a terminal of the exciting coil 11a on the side of the power source line 13 by detecting a voltage between the terminal of the exciting coil 11a and the output terminal 2a. The terminal open detection circuit 4a is constructed with voltage divider circuits 44 and 45 and a comparator 46. The voltage divider circuit 44 is constructed with series connected resistors R1 and R2 provided between the output terminal 2a and ground (GND). The voltage divider circuit 45 is constructed with series connected resistors R3 and R4 having one end connected to the power source line 13 through a terminal 2i and the other end grounded.

A (+) input of the comparator 46 is connected to a connecting point of the resistors R1 and R2 of the voltage divider circuit 44 and supplied with a divided voltage Va. A (-) input of the comparator 46 is connected to a connecting point of the resistors R3 and R4 of the voltage divider circuit 45 and supplied with a divided voltage Vb. In this case, since, when the output of the power transistor 3 increases and reaches a predetermined drive current, the voltage of the output terminal 2a becomes a value corresponding to the current value, Va > Vb. At this time, the output of the comparator 46 is changed from "H" to "L". That is, the comparator 46 generates an output detection pulse ("L" is significant) showing a generation of output current (see Fig. 2d). This output detection pulse is a detection signal outputted by the terminal open detection circuit 4a and showing that the output terminal 2a and the other terminal of the exciting coil 11a are

connected. That is, the detection pulse shows that these terminals are not in open state. Therefore, when the detection pulse is not generated in a case where the power transistor 3 outputs the drive current, it indicates that these terminals are in open state.

As shown in Fig. 2(d), the divided voltage Vb is set to a voltage value, which is close to a voltage caused by a limit drive current and lower by 5% to 20% of the voltage caused by the limit drive current. In this manner, by determining whether or not the output terminal 2a is opened when the power transistor 3 outputs the drive current and determining whether or not the output terminal is opened when the voltage is close to the value corresponding to the limit drive current, the terminal open detection is hardly influenced by noise or instantaneous open during a period in which the drive current flows through the exciting coil.

[0009]

The circuit breaking detection circuit 4b is constructed with a comparator 4c and an octal counter 4d. The octal counter 4d receives clock signals CLK from a clock generator circuit 14 through a terminal 2h. A (+) input of the comparator 4c receives a comparative reference voltage VR from a reference voltage generator circuit 6, which is provided commonly for the single phase drive circuits 1a to 1d, and a (-) input thereof receives the detection voltage signal from the terminal open detection circuit 4a. An output of the comparator 4c is connected to a reset terminal R of the octal counter 4d. Incidentally, the output of the reference voltage generator circuit 6 can be regulated by, for example, laser trimming. The voltage VR is set such that, by this regulation, the comparators 4c of the

single phase drive circuits 1a to 1d generate reset signals.

Incidentally, the reset signal is a falling edge of the output pulse of the comparator 4c, which is obtained when the output of the comparator 46 becomes "H" again after it falls to "L".

In response to the detection voltage signal from the terminal open detection circuit 4a, the circuit breaking circuit 4b detects a circuit breaking on the basis of a constant time period, for which the open state continues, by counting clocks by the octal counter 4d. That is, the circuit breaking detection signal is generated when the counting of the octal counter 4d (counting out of 8 clocks or more) is ended. Therefore, the circuit breaking detection signal is generated in a period in which the power transistor 3 is not outputting the drive current. Therefore, the circuit breaking detection signal is not influenced by noise during the power transistor 3 is operating.

A period TG of the gate drive pulse for driving the power transistor 3 is $TG < 8 \times T$, where T is the period of the clock CLK. In this embodiment, the time period TG is set to about 6 counts ($6 \times T$) of the octal counter 4d.

The comparator 4c supplies a "H" output pulse (reset pulse) to the octal counter 4d to reset the latter only when the comparator 46 generates the output detection pulse in "L" level. Therefore, the octal counter 4d starts the counting from "0". The output current of the power transistor 3 is generated by a next gate drive pulse, which is generated before the time $8 \times T$ elapses. So long as the output current is generated, the octal counter 4d is continuously reset. As a result, there is no 8 count end signal of the octal counter 4d

is not generated.

[0010]

When a circuit breaking occurs in a circuit from the terminal of the exciting coil 11a on the side of the power source line 13 to the output terminal 2a, the divided voltage of the voltage divider circuit 44 becomes ground potential. Therefore, when there is no output current generated by the power transistor 3, the output detection pulse generated by the comparator 46 is kept "H" even if a gate drive pulse is generated (see a later half wave in Fig. 2(e)). Therefore, the output pulse (reset pulse) of the comparator 4c is kept "L" and the octal counter 4d is not reset by the output pulse of the comparator 4c. As a result, the 8 count end signal of the octal counter 4d is generated when the power transistor 3 does not generate the output current. The 8 count end signal is the circuit breaking detection signal.

A reference numeral 41 depicts a drive stop signal generator circuit constructed with an OR gate 42 and a latch circuit 43. The latch circuits 43 receive the 8-count end signals "H" of the last stages of the octal counters 4d of the single phase drive circuits 1a to 1d as the circuit breaking detection signals through the OR gates 42. Thus, the latch circuits 43 receive the 8-count end signals "H" as "1" to latch the OR signals for the exciting coils 11a to 11d according to the clock CLK.

When the circuit breaking detection signal ("1") is latched, the latch circuit 43 supplies the "1" to the phase exciting signal generator circuit 9 as a drive stop signal SP, upon which the phase exciting signal generator circuit 9 stops its operation. Incidentally, when a reset signal "1" is

inputted to a reset terminal R of the latch circuit 43 through the terminal RS, the latch circuit 43 is cleared. In an initial state, the latch circuit 43 is set with "0" by this reset signal.

When a circuit breaking occurs in a circuit from the terminal of the exciting coil 11a on the side of the power source line 13 to the output terminal 2a, the octal counter 4d generates the 8-count end signal ("H") as the circuit braking detection signal and the "1" is latched by the latch circuit 43, so that the operation of the phase exciting signal generator 9 is stopped. Therefore, the stepping motor driver IC 10, particularly, the power transistor 3 thereof is not broken.

Incidentally, the circuit breaking detection signal may be an overflow signal or a carry signal of the octal counter 4d.

[0011]

The current limit circuit 5 is constructed with a comparator 5a and a reference voltage generator circuit 5b. A (+) input terminal of the comparator 5a is connected to a terminal 2f. The reference voltage generator circuit 5b is provided externally of the IC and connected to a (-) input terminal of the comparator 5a through a terminal 2g. Thus, a reference voltage VREF is applied to the (-) input terminal. Assuming that the terminal voltage (voltage at the terminal 2f) of a resistor Rs for detecting the output current is Vs, the comparator 5a generates a detection pulse S when the drive current (output current) of the power transistor 3 and the voltage Vs exceeds the reference voltage VREF, that is, when the output current reaches a rated value. The detection pulse S is supplied to a chopping pulse generator circuit 7 to turn "H" chopping pulse OFF ("L") and to drive an OFF timer circuit

8. Thus, the power transistor 3 is turned OFF (an operation of this will be described later).

A stop time ("L" period) of the chopping pulse P is counted by the OFF timer circuit 8 for setting the OFF time and, after a constant time, for example, 15msec, the chopping pulse P returns to "H". The chopping pulse P is "H" for a time selected within a range 30msec to 50msec. That is, the chopping pulse P, which is "H", becomes "L" according to the detection pulse S and, after the constant time, becomes "H".

As a result, the current limiting circuit 5 limits the output current of the power transistor 3 by stopping the drive current when the terminal voltage Vs of the resistor Rs exceeds the reference voltage VREF. In this point, the current limiting circuit 5 also works as an over-current protective circuit.

[0012]

The chopping pulse P, which is normally "H", is supplied to a phase exciting signal generator circuit 9. In the phase exciting signal generator circuit 9, the chopping pulse P is ANDed with a gate drive pulse "H" of, for example, the single phase drive circuit 1a and outputted to the gate of the power transistor 3 (see Fig. 2(a) and 2(b)). That is, the phase exciting signal generator circuit 9 supplies a chopping pulse (corresponding to the chopping pulse P) for cutting the power transistor OFF at a predetermined frequency to the power transistor 3 during the time for which the gate drive pulse is "H". When the chopping pulse P is "L", the gate drive pulse becomes "L", so that the power transistor 3 is in OFF state and the drive current of the exciting coil 11a of the stepping motor 11 is cut.

Since the flywheel diodes D are provided in parallel to

the exciting coils 11a to 11d, respectively, currents of the exciting coils flow through the flywheel diodes D, respectively, during the OFF period ("L" period) of the chopping pulse P. The current flowing through the diode D becomes an average current determined according to the ON period and the OFF period of the chopping pulse).

[0013]

The chopping pulse generator circuit 7 and the OFF timer circuit 8 are commonly provided for the single phase drive circuits 1a to 1d. and the chopping pulses P corresponding to the driving of the exciting coils of the single phase drive circuits 1a to 1d are generated, respectively, and supplied to the phase exciting signal generator circuit 9.

The phase exciting signal generator circuit 9 generates the "H" and "L" gate drive pulse of the power transistor 3 of each of the single phase drive circuits 1a to 1d according to the single phase drive, the single - two phase drive or the two phase drive, etc., of each exciting coil with a predetermined timing. Further, in order to limit the drive current, the "H" period of each gate pulse is chopped by the chopping pulse P. Incidentally, the period of the chopping pulse P is shorter than the period of the clock signal CLK.

[0014]

Fig. 2 is a timing chart of the operation of the power transistor protective circuit 4.

Fig. 2(a) shows the gate drive pulse of the single phase drive circuit 1a. The power transistor 3 is driven during the gate drive pulse is in "H" state. Fig. 2(b) shows the chopping pulse P. Since the drive current flows through the exciting coil 11a of the stepping motor 11 during the "H"

period of the chopping pulse P, an output voltage Vout of the output terminal 2a becomes as shown in Fig. 2(c).

It is assumed that the output current of the power transistor 3 of the single phase drive circuit 1a is generated correspondingly to the gate drive pulse shown in Fig. 2(a). In such case, since the output of the comparator 46 is changed from "H" to "L" when the divided voltage Va exceeds the divided voltage Vb (see Fig. 2(d)), the output pulse of the comparator 46 becomes the output detection pulse, which takes "H", "L", "H" and "L" correspondingly to the voltage Vout of the output terminal 2a shown in Fig. 2(c), as shown in Fig. 2(e). Since the period of the chopping pulse P is shorter than that of the clock pulse CLK, the comparator 4c resets the octal counter 4d by generating "H" output (reset pulse) correspondingly to the output detection pulse "L" of the comparator 46. Therefore, the latch circuit 43 is kept at the initial value "0" and the phase exciting signal generator circuit 9 continuously operates without generating the drive stop signal SP.

[0015]

The last output detection pulse "L" of the comparator 46 is generated correspondingly to the chopping pulse P immediately before the gate drive pulse shown in Fig. 2(a). A next output detection pulse "L" of the comparator 46 corresponds to an initial chopping pulse generated next. A period of the output detection pulse "L" of the comparator 46 is shorter than the period 8 x T for which the octal counter 4d counts 8 clocks. Therefore, so long as there is no breaking from the terminal of the exciting coil 11a on the side of the power source line 13 to the output terminal 2a, the latch circuit 43

does not generate the drive stop signal SP for the phase exciting signal generator circuit 9. Incidentally, it is enough that the count period of the octal counter 4d is equal to or longer than the period from the last output detection pulse to the next initial output pulse.

On the other hand, when there is any breaking in the circuit from the terminal of the exciting coil 11a on the side of the power source line 13 to the output terminal 2a due to defective connection to the stepping motor 11, the output current is not generated even when the power transistor 3 of the single phase drive circuit 1a is driven correspondingly to the gate drive pulse. Therefore, the voltage Vout of the output terminal 2a as shown in the later half of Fig. 2(c), resulting in that the divided voltage Va becomes Va nearly egual to 0V.

[0016]

As a result, Va < Vb and the output detection pulse generated by the comparator 46 is kept in "H". Therefore, the octal counter 4d is not reset and counts the clocks continuously. When there is no next output current generated, the comparator 46 does not generate the output detection pulse "L". Therefore, an 8 count end signal ("H") is generated by the octal counter 4d and latched in the latch circuit 43 as "1" through an OR gate 42. Therefore, the operation of the phase exciting signal generator circuit 9 is stopped, so that the stepping motor driver IC 10 is not destroyed.

In such case, it is preferable that a period of the 8 count end signal (circuit breaking detection signal) from the octal counter 4d is equal to or longer than a period in which a plurality of the output detection pulses "H" are generated by the comparator 46. In this embodiment, the period till the 8

count end of the octal counter 4d is set to a time longer than the period of the gate drive pulse of each of the single phase drive circuits 1a to 1d. Therefore, it is possible to continuously detect that the terminal open state continues for a time equal to or longer than the period of the gate drive pulse.

Incidentally, since the OR gate 42 receives an OR of the 8 count end signals (circuit breaking detection signals) obtained from the last stages of the octal counters 4d of the single phase drive circuits 1a to 1d, the operation of the phase exciting signal generator circuit 9 is stopped by the 8 count end signal from any of the octal counters 4d of the single phase drive circuits 1a to 1d.

[0017]

In the described embodiment, the time from the resetting to the count end of the octal counter 4d is 8 X T and the period TG of the gate drive pulse is 6 X T. And, when the detection signal indicating the connection state of the terminal open detection circuit 4a is not generated once, it is decided by the circuit breaking detection circuit 4b as a generation of the terminal open detection signal.

In the present invention, however, the octal counter 4d may be replaced by a terdenary counter or a more notation counter. In such case, when a plurality of the detection signals indicating the connection state of the terminal open detection circuit 4a are not generated continuously, it is decided that a plurality of the terminal open detection signals are continuously generated and the circuit breaking detection circuit 4b decides a circuit breaking. Thus, it is possible to reliably decide the circuit breaking.

In other words, it is possible, in the present invention, to decide the circuit breaking by setting the time from the resetting to the count end of the counter 4d longer than twice of the gate drive pulse period TG.

Incidentally, the circuit breaking detection circuit 4b may decide a circuit breaking by detecting a plurality of the terminal open detection signals even if these signals are not detected continuously.

[0018]

In the described embodiment, the comparator 5a is provided for each of the single phase drive circuits 1a to 1d. However, the comparator 5a may be provided for a plurality of the single phase drive circuits 1a to id. In such case, for example, a comparator 5a for the single phase drive circuits 1a and 1b and a comparator 5a for the single phase drive circuits 1c and 1d may be used by using the detection resistor Rs in common.

Further, although, in the described embodiment, the comparator 5 has two (+) input terminals, the internal circuit thereof may be constructed with two comparators connected in parallel. Alternatively, a comparator having two (+) input terminals and two (-) input terminals may be used.

Further, although, in the described embodiment, the circuit breaking detection signal is the count end signal of the octal counter, it is not always necessary to use the count end signal. The circuit breaking detection signal in this invention may be generated after the period from the output of the drive signal when the detection signal of the terminal open detection circuit is received to the output of the next drive current.

Although, in the described embodiment, the power transistor 3 is the MOSFET, a bipolar transistor may be used as the power transistor.

Further, although the motor drive circuit for driving the unipolar drive stepping motor driver IC has been described, it is of course possible to apply the present invention to a bipolar drive (positive and negative phase drive) stepping motor driver IC by using the output circuit of the power transistor as a push-pull drive circuit.

INDUSTRIAL APPLICABILITY

[0019]

Although, in the described embodiment, the power transistor 3 is OFF controlled through the chopping pulse generator circuit 7 and the OFF timer circuit 8, the chopping pulse generator circuit 7 and the OFF timer circuit 8 are not always necessary when a construction for OFF controlling the power transistor 3 is used.

Further, although the stepping motor driver IC has been described, the present invention is applicable to any drive circuit so long as the drive circuit has a current limiting circuit for limiting the drive current by the OFF control of the power transistor by using a rated current.

BRIEF DESCRIPTION OF THE DRAWINGS

[0020]

[Fig. 1] Fig. 1 is a block diagram showing an embodiment of a unipolar drive stepping motor driver to which a power transistor protective circuit of a motor drive circuit of the present invention is applied.

[Fig. 2] Fig. 2 is a timing chart of an operation of the power transistor protective circuit.

DESCRIPTION OF REFERENCE NUMERALS AND SIGNS

[0021]

1a,1b, 1c, 1d ··· single phase drive circuit

2a, 2b, 2c, 2d ··· output terminal

3 ··· N channel MOSFET power transistor

4 ··· power transistor protective circuit

4a ··· terminal open detection circuit

4b ··· circuit breaking detection circuit

4c, 46 ··· comparator

4d ··· octal counter

5 ··· current limiting circuit

5a ··· comparator

6 ··· reference voltage generator circuit

7 ··· chopping pulse generator circuit

8 ··· OFF timer circuit

9 ··· phase exciting signal generator circuit

10 ··· stepping motor driver IC

11a, 11b, 11c, 11d ··· exciting coil

12 ··· power source

13 ··· power source line

14 ··· clock generator circuit

41 ··· drive stop signal generator circuit

42 ··· OR gate

43 ··· latch circuit

44, 45 ··· voltage dividing resistor circuit

Rs ··· resistor

D ··· flywheel diode